IN THE CLAIMS

Please amend the claims to read as indicated herein.

1. (currently amended) An apparatus ~~adapted~~ for supplying a plurality of clock signals, said apparatus comprising:

a set of clock signal circuits ~~adapted~~ for generating m clock signals of at least two different signal periods, with m being a natural number; and

a superperiod signal generating unit ~~adapted~~ for deriving, from a dedicated clock signal of said set of clock signals, a first superperiod signal~~, whereby the~~ having a signal period ~~of said first superperiod signal~~ that is a common multiple of the clock signals' signal periods.

2. (currently amended) The apparatus of claim 1, wherein one signal period of said first superperiod signal comprises n_i signal periods of ~~the~~ a respective i-th clock signal, whereby n_i is a natural number, and $1 \leq i \leq m$.

3. (currently amended) The apparatus according to claim 1, wherein at least some of said clock signal circuits comprise synchronization facilities ~~adapted~~ for synchronizing at least some of said clock signals to said first superperiod signal.

4. (currently amended) The apparatus of claim 2, further comprising a central facility ~~adapted~~ for programming or reprogramming the respective value n_i corresponding to the i-th clock signal, for any i with $1 \leq i \leq m$.

5. (currently amended) The apparatus of claim 2, further comprising a central facility ~~adapted~~ for programming or reprogramming at least one of:

the clock frequency of the i-th clock signal, for any i with $1 \leq i \leq m$, or

the respective value n_i corresponding to the i-th clock signal.

6. (currently amended) The apparatus according to claim 1, wherein the signal period of said first superperiod signal is ~~the~~ a lowest common multiple of the clock signals' signal periods.

7. (currently amended) The apparatus according to claim 1, wherein said superperiod signal generating unit comprises a ~~first~~ superperiod counter ~~adapted~~ for generating one superperiod of said first superperiod signal per n_j signal periods of said dedicated ~~j-th~~ clock signal.

8. (currently amended) The apparatus according to claim 1, wherein at least some of said clock signal circuits delay their respective clock signal in a way that at least some ~~of the~~ edges of ~~the~~ a respective clock signal coincide with edges of said first superperiod signal.

9. (currently amended) The apparatus according to claim 1, wherein at least some of said clock signal circuits comprise variable delay elements ~~adapted~~ for compensating ~~the~~ a relative phase delay between ~~the~~ a respective clock signal and said first superperiod signal.

10. (currently amended) The apparatus according to claim 1, wherein at least some of said clock signal circuits derive second superperiod signals from ~~the~~ respective clock signals and synchronize said second superperiod signals to said first superperiod signal.

11. (currently amended) The apparatus of claim 10, wherein

at least some of said clock signal circuits delay both their respective clock signal and ~~the~~ a respective second superperiod signal derived therefrom in a way that the respective second superperiod signal is in phase with said first superperiod signal.

12. (currently amended) The apparatus according to claim 10, wherein at least some of said clock signal circuits comprise ~~second superperiod counters adapted~~ a superperiod counter for generating one superperiod of ~~the~~ a respective second superperiod signal per n_i

signal periods of ~~the~~ a corresponding i-th clock signal.

13. (currently amended) The apparatus according to claim 12, wherein at least some of said clock signal circuits comprise counter initialization units that sample said first superperiod signal in accordance with the corresponding i-th clock signal in order to obtain a series of sampling values, and that perform an initialization of ~~the~~ a corresponding ~~second~~ superperiod counter in dependence on a signal transition of said sampling values.

14. (currently amended) The apparatus according to claim 10, wherein at least some of said clock signal circuits comprise phase detection units ~~adapted~~ for determining ~~the~~ a relative phase delay between ~~the~~ a respective second superperiod signal and said first superperiod signal.

15. (currently amended) The apparatus according to claim 14, wherein said phase detection units are realized by means of flip-flops, ~~whereby~~ wherein said first superperiod signal is applied to the flip-flop's clock input, and ~~whereby~~ wherein the respective second superperiod signal is applied to the flip-flop's data input, or vice versa.

16. (currently amended) The apparatus according to claim 10, wherein at least some of said clock signal circuits comprise variable delay elements ~~adapted~~ for compensating ~~the~~ a relative phase delay between ~~the~~ a respective second superperiod signal and said first superperiod signal.

17. (original) The apparatus according to claim 1, wherein at least some of said clock signal circuits comprise clock selection facilities that allow to select, besides the clock signal circuit's own clock signal, a clock signal of a remote clock signal circuit as an output signal of said clock signal circuit.

18. (original) The apparatus according to claim 1, wherein any clock signal of said set of clock signals is selectable as said dedicated clock signal.

19. (currently amended) The apparatus according to claim 7, wherein ~~at least one of said first and said second superperiod counters~~ said superperiod counter is a programmable superperiod counter, ~~whereby the~~ wherein a respective ~~counter period n_i~~ signal period n_j can be programmed or reprogrammed.

20. (original) The apparatus according to claim 1, wherein said clock signals are utilized in a DUT testing environment for at least one of providing stimulus signals to a DUT or receiving response signals from the DUT.

21. (currently amended) An automated test equipment comprising:

test circuitry ~~adapted~~ for testing ~~at least one~~ a DUT, said test circuitry being responsible for at least one of: providing stimulus signals to said ~~at least one~~ DUT, and receiving response signals from said ~~at least one~~ DUT;

an apparatus according to ~~claims~~ claim 1, ~~whereby~~ wherein said apparatus provides a plurality of clock signals to said test circuitry.

22. (currently amended) The automated test equipment of claim 21, wherein at least one of the clock frequency of ~~the~~ an i-th clock signal, for any i with $1 \leq i \leq m$, or ~~the~~ a respective value n_i corresponding to the i-th clock signal, for any i with $1 \leq i \leq m$, is adapted to the clock domains of the DUT.

23. (currently amended) Data processing system comprising an apparatus ~~adapted~~ for supplying a plurality of clock signals, said apparatus comprising

a set of clock signal circuits ~~adapted~~ for generating m clock signals of at least two different signal periods, with m being a natural number; and

a superperiod signal generating unit ~~adapted~~ for deriving, from a dedicated clock signal of said set of clock signals, a first superperiod signal, ~~whereby the~~ having a signal period ~~of said first superperiod signal~~ that is a common multiple of the clock signals' signal periods.

24. (currently amended) A method for supplying a plurality of clock signals, comprising the steps of

generating m clock signals of at least two different signal periods, with m being a natural number; and

deriving, from a dedicated clock signal of said set of clock signals, a first superperiod signal~~, whereby the~~ having a signal period ~~of said first superperiod signal~~ that is a common multiple of the clock signals' signal periods.

25. (currently amended) The method of claim 24, further comprising a step of synchronizing at least some of said clock signals to said first superperiod signal.

26. (currently amended) A software program or product, preferably stored on a data carrier, ~~for executing the steps of~~ that provides instructions for a processor to execute steps of:

generating m clock signals of at least two different signal periods, with m being a natural number; and

deriving, from a dedicated clock signal of said set of clock signals, a first superperiod signal~~, whereby the~~ having a signal period ~~of said first superperiod signal~~ that is a common multiple of the clock signals' signal periods~~,~~

~~when run on a data processing system such as a computer~~.